12-04-00

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PATENT
Docket No. DELTA-2k01

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of
Inventor(s): **Robert M. Zwicker**

WARNING: Patent must be applied for in the name(s) of all the actual inventor(s). 37 CFR 1.41(a) and 1.53(b).

For (title): **SYNCHRONOUS RECTIFIER CONTROLLER FOR POWER SUPPLY SYSTEMS WITH HIGH POSER SWITCH AND HIGH EFFICIENCY**

1. Type of Application

This new application is a(n) (check one applicable item below):

X Original
_ Design
_ Plant

WARNING: Do not use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. 371(c)(4) unless the International Application is being filed as a divisional, continuation or continuation-in part Application.

NOTE: If one of the following 3 items apply then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED.

_ Divisional
_ Continuation
_ Continuation-in-part (CIP)

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date November 28, 2000 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EF246721336US addressed to the : Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Ching-lu Lin
(Type or print name of person mailing paper)

(Signature of person mailing paper)

NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon to mailing. 37 CFR 1.10(b).

2. Benefit of Prior U.S. Application(s) (35 USC 120)

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

__ The new application being transmitted claims the benefit of prior U.S. application(s) and enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed Which Are Required For Filing Date Under 37 CFR 1.53(b) (Regular) or CFR 1.153 (Design) Application

__15__ Pages of specification
__5__ Pages of claims
__1__ Pages of Abstract
__7__ Pages of Drawings
__X__ formal
__ informal

WARNING: DO NOT submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted the Office. **Only one copy is required or desired.** Comments on proposed new 37 CFR 1.84. Notice of March 9, 1988 (1990 O.G. 57-62).

NOTE: "Identify indicia such as the serial number, group and unit, title of the invention, attorney's docket number, inventor's name, number of sheets, etc., not to exceed 2 3/4 inches (7.0 cm.) in which may be placed in a centered location between the side edges within three fourths inch (19.1 mm.) of the top edge. Either this marking technique on the front of the drawing is acceptable." Proposed 37 CFR 1.84 (1). Notice of March 9, 1988 (1090 O.G. 57-62)

4. Additional papers enclosed

_ Preliminary amendment
_ Information Disclosure Statement
_ Form PTO-1449
_ Citations
_ Declaration of Biological Deposit
_ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
_ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
_ Special Comments
_ Other

5. Declaration or oath

X Enclosed

executed by (*check **all** applicable boxes*)

X inventor(s).

_ legal representative of inventor(s) . 37 CFR 1.42 or 1.43

_ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached

_ this is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. *See item 13 below for fee.*

_ Not Enclosed.

WARNING: Where the filing is a completion in the U.S. of an International Application but where a declaration is not available or where the completion of the U.S. application contains subject matter in addition to the International Application the application may be treated as a continuation or continuation-in-part as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

_ Application is made by a person authorized under 37 CFR 1.41 (c) on behalf of *all* the above named inventor(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16 (e) can be filed subsequently.

NOTE: It is important that **all** the correct inventor(s) are named for filing under 37 CFR 1.41 (c) and 1.53 (b).

6. Inventorship Statement

WARNING: If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the **last** claimed invention was made, should be submitted.

The inventorship for all the claims in this application are:

X The same

or

_ Are not the same. An explanation, including the ownership of the various claims at the time the **last** claimed invention was made.

_ is submitted

_ will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. A verified English translation of the non-English language application and the processing fee of $30.00 required by 37 CFR 1.17(k) is required to be filed with the application or within such time as may be set by the Office. 37 CFR 1.5(d).

NOTE: A non-English oath or declaration in the form provided or approved by the PTO need not be translated. 37 CFR 1.69(b).

X English

_ non-English

_ the attached translation is a verified translation. 37 CFR 1.52(d).

8. **Assignment**

X An assignment of the invention to Delta Electronics, Inc.

X is attached

_ will follow

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment" Notice of May 4, 1990.

9. Certified Copy

Certified cop(ies) of application(s)

(country) (appl.no.) (filed)

from which priority is claimed

_ is (are) attached . A separate "ASSIGNMENT COVER LETTER ACCOMPANYING NEW PATENT APPLICATION" is also attached

_ will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37CFR 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35USC120 is itself entitled to priority from a prior foreign application then complete item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10 Fee Calculation (37 CFR 1.16)

A X Regular application

CLAIMS AS FILED				
Number filed	Number Extra		Rate	Basic Fee $710.00
Total				
Claims 37 CFR 1.16(c)	15-20 = 0	x	$18.00	0.00
Independent				
Claims (37CFR 1.16(b))	3 -3 = 0	x	$ 80.00	0.00
Multiple dependent claim(s), if any				
(37 CFR 1.16(d))			$270.00	0.00

_ Amendment Cancelling extra claims enclosed.

_ Amendment deleting multiple-dependencies enclosed.

_ Fee for extra claims is not being paid at this time.

note: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37CFR1.16(d).

Filing fee calculation $ 710.00

B. _ Design application
($310.00 - 37 CFR 1.16(f))

Filing fee calculation $_____

C _ Plant application
($510.00 - 37 CFR 1.16(g))

Filing fee calculation $_____

11. Small Entity Statement(s)

__Verified Statement(s) that his is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

Filing Fee Calculation (50% of **A, B,** or **C** above) $_____

NOTE: any excess of the full fee paid will be refunded if a verified statement and a refund request are filed within 2 months of the date of timely payment of a full fee. 37 CFR 1.28(a).

12. Request for International-Type Search (37 CFR 1.104(d)) (*complete, if applicable*)

_ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made At This Time

_ Not Enclosed

_ No filing fee is to paid at this time. (*This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.*)

X Enclosed

X basic filing fee $_____**710.00**

X recording assignment
($40.00; 37 CFR 1.21(h)) $_____**40.00**

_petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached.
($120.00; 37 CFR 1.47 and 1.17(h)) $_____

_ for processing an application with a specification in a non-English language. ($300.00; 37 CFR 1.52(d) and 1.17(k)) $_____

_ processing and retention fee
($130.00; 37 CFR 1.53(d) and 1.21(l))

_ fee for international-type search report
($40.00; 37 CFR 1.21(e)) $_____

NOTE: 37 CFR 1.21(l) establishes a fee for processing and retaining any application which is abandoned for failing to complete the application pursuant to 37 CFR 1.53(d) and this, as well as the changes to 37 CFR 1.53 and 1.78, indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid or the processing and retention fee of 1.21(l) must be paid within 1 year from notification under 53(d).

Total fees enclosed $ _____**750.00**

14. Method of Payment of Fees

X Check in the amount of $ 750.00

_ Charge Account No. in the amount of $_____. A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner the it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

15. Authorization to Charge Additional Fees

WARNING: if no fees are to be paid on filing the following items should not be completed.

WARNING: Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.

X The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 12-0005.

X 37 CFR 1.16(a), (f) or (g) (filing fees)

X 37 CFR 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 CFR 1.16(d)) it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

_ 37 CFR 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later then the filing date of the application)

_ 37 CFR 1.17 (application processing fees)

WARNING: While 37 CFR 1.17(a),(b) (c) and (d) deal with extensions of time under 1.136(a) this authorization should be made only with the knowledge that: "Submission of the appropriate extension fee under 37 C.F.R. 1.136(a) is to avail unless a request or petition for extension is filed." (Emphasis added). Notice of November 5, 1985 (1060 O.G. 27)

_ 37 CFR 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b))

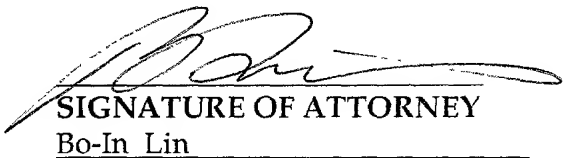
NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 CFR 1.311(b).

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application...prior to paying, issue fee". From the wording of 37 CFR 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions As to Overpayment

_ credit Account No.

X refund



Reg. No.**33,948** **SIGNATURE OF ATTORNEY**

Bo-In Lin

Tel. No. (415) 949-0418 Type or print name of attorney

P.O. Address : **13445 Mandoli Drive,**
Los Altos Hills, CA 94022

__ **Incorporation by reference of added pages**

Check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR A NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED

_ Plus Added Pages For New Application Transmittal Where Benefit Of Prior U.S. Application(s) Claimed
Number of pages added _____

_ Plus Added Pages For Papers Referred To In Item 4 Above
Number of pages added _____

_ Plus "Assignment Cover Letter Accompanying New Application"
Number of pages added _____

X Statement Where No Further Pages Added

(If no further pages form a part of this Transmittal then end this Transmittal with this page and check the following item)

X This transmittal ends with this page

SYNCHRONOUS RECTIFIER CONTROLLER FOR POWER SUPPLY SYSTEMS WITH HIGH POWER SWITCH AND HIGH EFFICIENCY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to AC-to-DC converter systems. More particularly, this invention relates to an improved controller circuit design and configuration for use with synchronous rectification to achieve high power conversion efficiency.

2. Description of the Prior Art

Conventional art of design and manufacture of AC to DC converter systems is not able to satisfy the more advancing requirements now imposed by the high performance server technology. These requirements include smaller size, lower fan noise, high reliability, low cost and low power consumption. The power supply systems are now employed in the computer industries to convert various AC voltages ranging from one hundred to two hundred and forty volts to regulated DC voltages of 3.3, 5, 12 and –12 volts. Specifically, the difficulties arise from the facts that these requirements appear to constrain the designs of the power supply systems in opposite directions. On the one-hand the power supply is expected to produce more output power and be more reliable. On the other hand, the power supply is constrained by seemingly contradictory requirements that the system be made smaller, quieter, and cheaper. One of the best ways to satisfy these requirements is to increase the efficiency of the power supply system. This is because efficiency improvement would lead to reduction of heat generation thus allow for smaller size of a power supply to operate at a lower temperature that would increase the reliability and meanwhile require less noise generated by fans for heat-dissipation. Although, there may be a concern that a system designed for higher efficiency tends to be more complex, and this increases the production cost, such concerns are likely offset by the follow-on savings

in heat dissipation, package, shipping, and cost reductions resulted from lower power consumption.

There are a number of ways to increase the efficiency of a power supply. A method is to reduce the losses in the output rectifier of a converter since these losses are relatively large compared to other losses. In a high frequency power converter as that shown in Fig. 1A, the standard devices for rectifying an output voltage of three to five volts are schottky diodes D1 and D2. Fig. 1A is a generic representation of a basic forward converter showing a conventional circuit configuration of forward switching converter for a power supply system operated with a pulse width modulator controlling a main switching transistor Q1 at the primary side. The Pulse Width Modulator is any one of many commercial integrated circuits, which can modulate a pulse width duty cycle based upon a feedback signal. Its output is an approximately 0 to 12V pulse waveform at a fixed frequency, e.g., a frequency of 100 KHz. This waveform drives the main switching transistor Q1. Transistor Q1 acts as a power switch under control of the Pulse Width Modulator output. With a rectified input voltage source 400 volts DC, the waveform appearing at the output (drain) of Q1 has a peak value of about 400 Volts or a peak-to-peak value of 800 Volts. The primary side is coupled to the secondary side with a transformer T1 with the secondary side provided with rectifying diodes D1 functioning as a forward output diode and D2 as a freewheel output diode. The output load is coupled in series with an output filter inductor and in parallel to an output filter capacitor. For a typical 5 Volt DC output, the transformer has a turns ratio defined by Np : Ns of about 15:1 where Np is the number of turns of the primary side and Ns is the number of turns of the secondary side. The peak voltage into the anode of D1 is around 25 Volts. When Q1 is on, D2 is reverse biased and D1 is forward biased (the anode is positive relative to the cathode). During this time, a positively sloped output current flows through D1 and L1 to the output load. L1 (output filter inductor) stores most of the transformer output energy pulse to produce a ramping current which is usually continuous. When Q1 is off, D1 is reverse biased and L1 maintains a negatively-ramping current by forward-biasing D2 as it discharges some

of its stored energy. Except for resistive losses, the average voltage across C1 is identical to the average voltage across D2. C1 serves to filter the periodic and random perturbations from the DC output voltage so as to reduce them to acceptable levels.

As that shown in Fig. 1A, Schottky diodes often cause a forward voltage drop of about 0.6 volts. Even if the power supply has no other losses, the voltage drops caused by the shottky diodes represent about ten to fifteen percent efficiency loss for a three to five volt output. In order to compensate for these losses, higher power is required prior to a rectification action taken by the schottky diodes. A higher power processed by prior stages of the power supply system tends to increase losses further during during these prior-stage-processing functions. As a result, the losses are compounded and the total efficiency losses are significantly increased. Conversely, the total power savings achieved by improving the output rectifier efficiency tend to have a reverse effect of compounding the improvement of the efficiency for the entire power supply system. There are methods to incrementally minimize the losses of the schottky diodes by optimizing the transformer and choosing the best schottky diodes. However, improvements of power losses achievable by using better schottky diodes are quite limited. Under the circumstances when a small performance improvement is required, better schottky diodes would generally be sufficient to satisfy the requirement. But when compared to another technique of applying a synchronous rectification, even the best schottky diodes would come short of matching the performance when synchronous rectification is employed for AC to DC conversion.

An effective method to increase the output rectifier efficiency is by implementing a controlled switch to achieve synchronous rectification. In the recent past, synchronous rectification was considered too exotic for commercial applications. The device most commonly used for the controlled switch is a MOSFET. Advancement in semiconductor technology has improved the cost/performance of the MOSFETs, and the power supply industry now begun to use synchronized rectification for

performance improvement as the improvements achievable by the schottky are not sufficient to meet the demand of higher performance. The most commonly available switch is an n-channel MOSFET transistor that has an operation characteristic of providing a blocking voltage when the drain is positive relative to the source and the gate is at a zero or negative potential relative to the source. Due to an inherent drain-to body diode, there will be always a current even under a negative gate biased condition when the drain is negative relative to the source. This is normally considered as an undesirable feature for typical applications of the n-channel MOSFET. However, by providing a positive voltage to the gate, e.g., 10 volts relative to the source to turn on the n-channel MOSFET, the n-channel MOSFET will conduct a current with a very low voltage drop. This occurs regardless of the polarity of the voltage applied to the drain relative to the source. The MOSFET transistor thus provides an operation characteristic that is useful to function as a very efficient rectifier. Specifically, the rectifying function is achieved by adjusting the gate-source voltage to negative or zero to prevent a reverse current. And, conversely to generate a low voltage-drop conducting condition by adjusting the gate-source voltage to positive to provide a rectified current. The method is however depends on proper synchronization of the gate voltage to the variations of the relative source-drain potential. Fig. 1B shows a conventional synchronous rectified converter where the synchronization control signal is generated from the primary side. Specifically, a leading dead time (referring to Fig. 3 below) is generated from the control signals for Q1 and applied simultaneously to the synchronous rectifier switching transistor Q2 through a driver circuit. The pulse width modulation output is transmitted across the safety isolation barrier to driver circuit using a transformer or other device with a delay inserted between the PWM signal and main switch Q1 on the primary side. Such control scheme for achieving synchronous rectification has the disadvantages that it is necessary to provide an added signal path across the isolation barrier and usually that requires a bulky and expensive transformer. Also, the circuit of the primary circuit must be modified in order to accommodate this control scheme and that adds to the production cost of the power supply systems. Other than these

considerations, the control method using synchronous rectification is employed in high efficiency non-isolated DC-DC converters commonly used to power the central processor unit (CPU) of a computer. However, due to above difficulties and considerations, and the facts that conventional power supply systems can usually tolerate lower efficiency, synchronous rectification is usually not employed in off-line power supply system for AC-DC conversions.

For the above reasons, a need still exists in the art of designing and manufacturing a power supply system with voltage rectifying converter to provide an improved apparatus and method to increase the efficiency of the rectifying operations. Specifically, an improved method to improve the synchronous rectification of a power supply system to achieve lower voltage drop with precise time control of gate voltage synchronization is required to overcome the difficulties and limitations faced by those of skill in the art of the power supply industry.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide a novel and improved AC/DC converter to achieve a lower voltage drop for increasing the rectification efficiency with better cross regulation such that the more advanced requirements imposed on a power supply for high-performance servers can be satisfied.

Specifically, a synchronized rectification controller is employed to control a synchronized rectification (SR) switch implemented on the secondary side of the AC/DC converter. The SR switch is implemented as a MOSFET with synchronization rectifier controller control the sequence and timing of the gate voltage of the SR MOSFET in response to the switching on and off of the transformer and the voltage variations of the rectifier diodes used in the AC/DC converter. By precisely controlling the gate voltage of the SR MOSFET to assure an operation of synchronized rectification, higher conversion efficiency is achieved with lower voltage drops and power losses resulted from the AC/DC conversion process.

Another object of this invention is to provide improved synchronous rectification circuit configuration with new control circuit. The new control circuit allows the addition of synchronous rectification to the non-post regulated output of the power supply without any modifications to the transformer or the control of the primary side of the power supply and without any additional bridging to cross over the primary-secondary barrier.

Another object of this invention is to provide improved synchronous rectification circuit configuration with new control circuit to perform the necessary functions with inexpensive, commonly available parts as required circuit elements. The performance improvements are therefore achieved without unduly increasing the production cost of the power supply system.

Briefly, this invention discloses an AC-to-DC converter that includes a transformer having a primary side for inputting an input signal and a secondary side for outputting an output signal. The AC-to-DC converter further includes a synchronous rectifier controller connected to the secondary side for controlling a synchronous rectifier (SR) switch on the secondary side for generating the output signal. The SR switch is implemented as a MOSFET transistor with a gate connected to the synchronous rectifier controller. The synchronous rectifier controller further includes a plurality of circuit elements for turning off the SR switch before a main switch of the transformer is turned on. The synchronous rectifier controller further turns on the SR switch when the main switch of the transformer is turned off. The synchronous rectifier controller controls the SR switch and turns it off with a precisely controlled dead time before the main switch of the transformer is turned on.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment which is illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows the circuitry configuration of a conventional AC/DC converter implemented with basic forward switching topology;

Fig. 1B shows a prior art synchronous-rectified AC/DC converter implemented with a primary side control;

Fig. 2 shows the circuitry configuration of a forward AC/DC converter with synchronous rectifier controller of this invention with a synchronous switching control driver on the secondary side;

Figs. 3A to 3E show the timing sequences of the operational characteristics of the converter according to a circuit configuration shown in Fig. 2;

Fig. 4 is a functional block diagram showing a desired new function block of this invention on the secondary side to generate the synchronous rectifying actions by controlling a driver circuit to drives a SR switching transistor Q2;

Figs. 5A and 5B are block diagrams for illustrating different functional blocks necessary to carry out this invention;

Fig. 6 is a specific circuit implementation of the block diagram shown in Figs. 5A and 5B; and

Fig. 7 shows the variations of voltages over time at different points of the synchronous rectifier controller relative to the transformer output; and

Fig. 8 shows an enabling and disabling timing diagram according to a circuit implemented as that shown in Figs. 5A to 6.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 2 for a forward converter with synchronous rectifier controller of this invention for controlling a synchronous rectifier

(SR) switch S1. The control circuit and the method to generate a leading dead time will be further discussed below. Figs. 3A to 3E show the timing sequences of the operational characteristics of this converter according to a circuit configuration shown in Fig. 2 to achieve the synchronous rectification. The pulse width modulation as that shown in Fig. 2 is provided to generate a pulse width duty cycle of Fig. 3A based on a feedback signal. The output from the pulse width modulator is an approximate 0 to 12 volts pulse waveform at a fixed frequency, e.g., 100 KHz. The pulse width modulator controls a transistor Q1 that functions as a main switch on the primary side. When the output of the pulse width modulator is high, Q1 switches into an ON state with low resistance and forces one end of the transformer at the primary winding to a voltage near zero (Fig. 3B). With a voltage of 400 volts applied to the remote end of the transformer primary winding, the full 400V input is applied across the winding. When the output of the pulse width modulator is low, the transistor Q1 switches into an OFF state with a very high resistance to allow the transformer primary winding voltage to reset to a voltage near 800 volts. This voltage is normally controlled with a clamp circuit that is not discussed in this Application because it is not the main theme of this invention. After the transformer resets, the voltage across all windings drifts toward zero with a damped sinusoidal waveform and that is illustrated as the curved portion of the waveform of Fig. 3B. In response to the changes of the drain voltage of the transistor Q1, the voltage variations of the transformer output to D1 anode is shown in Fig. 3C and the D1 cathode output voltage is shown in Fig. 3D. Fig. 3E shows the voltage waveform applied to the synchronous switch SR gate. Fig. 3E shows the requirements of a leading dead time to turn off the S1 before the main switch Q1 on the primary side is turned on and a lagging dead time to turn on the S1 after Q1 is turned off.

Instead of applying a conventional method to generate the control signals for providing the leading and lagging dead time control from the primary side as discussed above for Fig. 1B, a novel circuit configuration is implemented as that shown in Fig. 4. A "desired new function" block is illustrated on the secondary side to generate the synchronous rectifying

actions by controlling a driver circuit that drives a SR switching transistor Q2. The driver circuit employs the output on the secondary side from the transformer T1 and a diode D1 to control the gate of a MOSFET switching device implemented as synchronous rectifier switch Q2.

Referring to Fig. 5A for a block diagram and Fig. 6 for a specific circuit implementation of the block diagram shown in Fig. 4. Fig. 5B shows the waveforms for the variations of voltage over time at different points of the circuit as processed by different functional blocks of Fig. 5A implemented according to Fig. 6. The output from the secondary winding 105 is inputted to a synchronous rectifier controller 100 that includes a waveform clipper 105 implemented with diode D952, resistor R994 and transistor Q958 and these circuit elements are employed to square up the input timing waveform from the +5 output rectifier. The waveform received from the secondary winding input 105 may have anomalies that can cause the dead time generator to malfunction. The waveform clipper 110 serves to minimize the anomalies such that the waveform is more closely approximated to a clean rectangular waveform. The signals processed by the waveform clipper 110 is transmitted to a pulse differentiator 115 implemented with C958 and R979 to produce a narrow pulse corresponding to the turn-on of the main switch transistor. The purpose of the differentiation is to provide immunity from the variable turn-off time of trailing edge-modulated main transformer waveform. A stable pulse is generated and used by a timing ramp generator 125 to synchronize and reset and re-trigger the timing ramp. The timing ramp generator 120 implemented with IC951:1, R973, R974, R975, R976, R977, R978, C956, and C957 to produce a positive-sloped ramp that is reset and then re-initiated by the pulse from the differentiator 115. The timing ramp resets and restarts when the main switching transistor turns on. In a fixed frequency, trailing edge-modulated converter, the controller operates normally and the timing should not vary regardless of the variations of the input voltage or the output load. With each pulse from the differentiator 115, the ramp voltage is reset to the same low voltage and begins to ramp up according to an R*C time constant of the resistor R973 and capacitor C956.

A pulse width generating comparator 125 compares the ramp voltage generated by the timing ramp generator 120 with the voltage of the charge integrator 135 implemented with a resistor R957 and capacitor C951. When the timing ramp voltage raises above the voltage on the charge integrator 135, the signal from the pulse width generating comparator 125 transmitted to the output driver is forced to a low voltage. And, the positive current source 130, implemented with transistor Q951, resistors R951, R952, and 953, is turned on. The positive current source 135 applies a fixed charge current to the charge integrator 135 whenever the output of the pulse width generating comparator 125 is low and the output of the transformer winding voltage dependent switch is high. In normal steady state operation, the voltage on the charge integrator 135 settles at an equilibrium voltage such that the current in the discharge resistor R957 equals to the average output of the positive current source that can be represented by a current set-point multiplied by the duty cycle. To achieve the purpose of synchronous rectification control, two transistors Q952 and Q953 are implemented as the transformer winding voltage dependent switches 140 and 145 respectively. The switch 140 implemented by the transistor Q952 disables the current source 130 whenever the main switching transistor is turned on and the transformer output voltage is high. Meanwhile the second voltage controlled switch 145 implemented with transistor Q953 forces the signal to the output driver 150 low under the same condition, specifically when the main switching transistor is turned on and the transformer output voltage is high. The output driver 150 is connected to the gate of the synchronous rectifier FET 160 while the drain of the FET 160 is connected to the secondary winding input 105.

When the normal operation begins, the voltage on the charge integrator 135 is close to zero volts. The timing ramp voltage generator 120 has a voltage surpasses the voltage on the charge integrator 135 early in the operation cycle. A large dead-time signal is generated to quickly turn off the gate of the synchronous rectifier MOSFET 160 thus causes a long duration pulse of current from the positive current source 130 to raise the voltage on the charge integrator 135. The pulse is terminated

when the transistor Q952 is turned on. With the increase in the voltage on the charge integrator 135, the dead time in the next cycle is shortened. This operational sequence continues as the voltage on the charge integrator 135 and the dead time settle exponentially to a stabilized equilibrium value. Adjusting the value of the positive current source 130 and the discharge resistor of the charge integrator 135 can program and tune the equilibrium value. With the circuit configuration shown in Figs. 5 and 6, excess dead time is generate to provide safety margin during the startup period of the power system until the operation is stabilized.

The synchronous rectifier controller includes an output current detector 180 to detect the output current. The synchronous rectifier (SR) switch must turn off when the inductor current approaches zero so that it does not conduct a reverse inductor current. This is achieved by disabling the SR MOSFET gate drive when DC output current is low. The sensing of output current with a current detector 180 is achieved by sensing the DC voltage drop across the output inductor. The terminal labeled inductor input in Fig. 6 has a pulse waveform and the output is a DC current. Ideally the inductor would integrate the waveform to produce a filtered DC output. However, the copper wire in the inductor has some DC resistance and the resistance when multiplied by the DC current produces a DC voltage drop. The terminal labeled with inductor output is connected to other end of the inductor. The potential difference between these two points is a large AC pulse waveform, typically more than 10 volts, and a small average DC voltage, typically less than 0.1 volts. For the function described above, the output current detection is not required to be highly accurate and the inductor-induced DC voltage is sufficiently accurate when proper filtering is applied and the voltage is detected by an IC voltage comparator. The first stage of filtering and detection is performed by the output current sensor 180 employing circuit elements IC951:4, C954, C955, R970, R971, and R972. An additional asymmetrical filtering and delay function performed by the delay timer 170 is implemented with circuit elements, R968 R967, and C953. The signal is provided to another comparator section IC951:3 that provides output and hysteresis to feedback to the previous comparator. The output of the

IC951:3 drives a transistor Q954 which discharges the charge integrator 135 in the dead time generator and that drives a transistor Q955 to force the gate drive output to a state of "low". The voltage variations over time at different points of the controller shown in Fig. 6 are depicted in Fig. 7. The output signal voltage variations produced by the current detector are generally much slower that those produced by the dead time generator. Thus a diagram showing the waveform will show many cycles of the ramp generator corresponding in time to one or two transitions from the current detector. By employing the circuit configuration described above, the synchronous rectifier controller is applied to properly control the gate of the MOSFET to achieve operation conditions as set forth specifically below:

1) The gate of the freewheel synchronous rectifier MOSFET must be turned "off" whenever the voltage on its drain is driven "high". If this is not assured and the gate of the freewheel synchronous rectifier MOSFET turns "on" when the voltage on its drain is driven "high", "cross conduction" current would flow. This wastes power, and any significant duration of this condition will probably destroy the power supply.

1a) In the main (+5) output with no magnetic amplifier, the voltage on the drain of the synchronous rectifier FET corresponds in time to the output of the primary switching transistor. Practical timing considerations require that the turn-off of the freewheel SR MOSFET gate be initiated before the turn on of the primary switching transistor. This anticipation is referred to as "dead time." This is because a small but significant time is required to transition the gate voltage from a fully "on" level to a fully "off" level. The cross conduction current which would result from this delay time postponing a reactively-triggered turn-off of the SR MOSFET gate would cause excessive power dissipation and possible voltage "spikes". The method of generating the anticipatory dead time is the unique aspect of this design.

1b) In the magnetic amplifier-regulated (+3.3) output, the timing considerations are easier. This is because the magnetic amplifier produces

a minimum delay time after the main switching transistor is turned on and before the drain of the freewheel SR MOSFET is driven "high". As a result, an "anticipatory" signal is readily available and the design of the controller for the 3.3V SR MOSFET gate is significantly simpler as a result.

2) The gate of the freewheel synchronous rectifier MOSFET must be turned "off" when the inductor current approaches zero. If this is not the case and the MOSFET is held "on" as the inductor current approaches zero, the inductor current will continue to transition increasingly negative, with this negative current flowing through the MOSFET. At some point the MOSFET must be turned off, and this negative inductor current can cause a destructive voltage spike in response. In practice, this situation can arise when the output is not heavily loaded.

3) The gate of the freewheel synchronous rectifier MOSFET must be turned "on" as much as possible when the primary switching transistor is turned "off" and significant output current is flowing through the output inductor. This is the purpose of the synchronous rectifier, and it is useless if it is not turned on as needed.

According to above time sequences of controlling the gate voltage by using the synchronous rectifier controller, Fig. 7 shows the variations of voltages over time at different points of the synchronous rectifier controller relative to the transformer output. Fig. 8 shows an enabling and disabling timing diagram according to a circuit implemented as that shown in Figs. 5A to 6. As described above, the timing ramp generator 120 (IC951) is applied to ramp up the voltage while the pulse generator comparator 125 compares the timing ramp voltage with the voltage on capacitor C951 of the charge integrator 135. Soon as the timing ramp voltage becomes higher than the voltage on capacitor C951 of the charge integrator 135, the transistor Q952 of the positive current source 130 becomes high. At that point in time, the voltage of the gate for the synchronous rectifier is driven to a low state. Therefore, precise control of the duration of the leading dead time is achieved to assure synchronous rectification is properly executed in synchronization with the switching

actions on the primary side and sufficient safety margins are also provided.

According to above drawings and description, this invention discloses a new AC-to-DC converter that includes a transformer having a primary side for inputting an input signal and a secondary side for outputting an output signal. The converter further includes a synchronous rectifier controller connected only to circuits on the secondary side for controlling a synchronous rectifier (SR) switch on the secondary side for generating the output signal. The SR switch includes a MOSFET transistor having a gate connected to the synchronous rectifier controller. The synchronous rectifier controller further includes a plurality of circuit elements for turning off the SR switch before a main switch of the transformer is turned on and for turning on the SR switch when the main switch of the transformer is turned off. The synchronous rectifier controller includes a dead-time means for generating a dead-time for turning off the SR switch with a controlled dead-time before the main switch of the transformer is turned on. The synchronous rectifier controller includes a pulse differentiator for generating a narrow pulse corresponding to a timing of a main switch of the transformer is turned on. The dead-time means further includes a time-ramping means initiated by the narrow pulse from the pulse differentiator for generating an up-ramping voltage. The dead-time means further includes a dead-time comparator for comparing the up-ramping voltage with a voltage generated by a charge integrator for generating a dead-time signal for turning off an output current driver. The charge integrator includes a circuit having a fixed time-constant of charge-integration independent of an output load of the AC-to-DC converter. The synchronous rectifier controller further includes a positive current detector for enabling a positive current source for providing a constant positive current to charge the charge integrator. The synchronous rectifier controller further includes a positive current switch for turning on and off the positive current source depending on an output of a secondary winding of the transformer.

In essence, this invention discloses a new synchronous rectifier controller for an AC-to-DC converter. The synchronous rectifier controller is connected only to circuits on a secondary winding of a transformer of the AC-to-DC converter. The synchronous rectifier is responding to a voltage of secondary winding for controlling a synchronous rectifier (SR) switch on the secondary side for generating a DC output signal. In a preferred embodiment, the SR switch comprising a MOSFET transistor having a gate connected to the synchronous rectifier controller. In another preferred embodiment, the SR switch comprising a N-channel MOSFET transistor having a gate connected to the synchronous rectifier controller for turning off the MOSFET when a drain of the N-channel MOSFET transistor is driven high.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alternations and modifications will no doubt become apparent to those skilled in the art after reading the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alternations and modifications as fall within the true spirit and scope of the invention.

CLAIMS

We claim:

1. An AC-to-DC converter comprising:

a transformer having a primary side for inputting an input signal and a secondary side for outputting an output signal;

a synchronous rectifier controller connected only to circuits on said secondary side for controlling a synchronous rectifier (SR) switch on said secondary side for generating said output signal;

said SR switch comprising a MOSFET transistor having a gate connected to said synchronous rectifier controller;

said synchronous rectifier controller further comprising a plurality of circuit elements for turning off said SR switch before a main switch of said transformer is turned on and for turning on said SR switch when said main switch of said transformer is turned off;

said synchronous rectifier controller comprising a means for generating a dead-time for turning off said SR switch with a controlled dead-time before said main switch of said transformer is turned on;

said synchronous rectifier controller comprising a pulse differentiator for resetting and restarting a ramp generator at a time when a main switch driving said transformer on;

said dead-time means further comprising a voltage-ramping means initiated by an output from said pulse differentiator for generating an up-ramping voltage;

said dead-time means further comprising a dead-time comparator for comparing said up-ramping voltage with a voltage generated by a charge integrator for generating a dead-time signal for turning off an output current driver.

said charge integrator comprising a circuit having a fixed time-constant of charge-integration independent of an output load of said AC-to-DC converter;

said synchronous rectifier controller further comprising an output current detector for enabling a positive current source for providing a fixed positive current to charge said charge integrator; and

said synchronous rectifier controller further comprising a switch for turning on and off said positive current source depending on an output of a secondary winding of said transformer.

2. An AC-to-DC converter comprising:

a transformer having a primary side for inputting an input signal and a secondary side for outputting an output DC signal; and

a synchronous rectifier controller connected only to circuits on said secondary side for controlling a synchronous rectifier (SR) switch on said secondary side for generating said DC output signal.

3. The AC-to-DC converter of claim 2 wherein:

said SR switch comprising a MOSFET transistor having a gate connected to said synchronous rectifier controller.

4. The AC-to-DC converter of claim 2 wherein:

said synchronous rectifier controller further comprising a plurality of circuit elements for turning off said SR switch before a main switch driving said transformer on and for turning on said SR switch when said main switch of said transformer is turned off.

5. The AC-to-DC converter claim 4 wherein:

said synchronous rectifier controller comprising a means for generating a dead-time for turning off said SR switch with a controlled dead-time before said main switch of said transformer is turned on.

6. The AC-to-DC converter claim 5 wherein:

said synchronous rectifier controller comprising a pulse differentiator for resetting and restarting the voltage ramp generator at a time when a main switch driving said transformer on.

7. The AC-to-DC converter claim 6 wherein:

said dead-time means further comprising a voltage-ramping means initiated by an output from said pulse differentiator for generating an up-ramping voltage; and

said dead-time means further comprising a dead-time comparator for comparing said up-ramping voltage with a voltage generated by a charge integrator for generating a dead-time signal for turning off an output current driver.

8. The AC-to-DC converter claim 7 wherein:

said charge integrator comprising a circuit having a fixed time-constant of charge-integration independent of an output load of said AC-to-DC converter.

9. The AC-to-DC converter claim 7 wherein:

said synchronous rectifier controller further comprising a positive current detector for enabling a positive current source for providing a constant positive current to charge said charge integrator; and

said synchronous rectifier controller further comprising a positive current switch for turning on and off said positive current source depending on an output of a secondary winding of said transformer.

10. The AC-to-DC converter of claim 3 wherein:

said SR switch comprising a N-channel MOSFET transistor having a gate connected to said synchronous rectifier controller for turning off said MOSFET when a drain of said N-channel MOSFET transistor is driven high.

11. The AC-to-DC converter claim 2 wherein:

said synchronous rectifier controller comprising a voltage clamp waveform clipper connected to an output of a secondary winding of said transformer for providing a square waveform corresponding to said output of said secondary winding.

12. The AC-to-DC converter claim 2 wherein:

said synchronous rectifier controller further comprising a current threshold detector connected to an output of a secondary winding of said transformer for sensing and turning off said SR switch when a current said output of said secondary winding is reduced below a threshold voltage.

13. A synchronous rectifier controller for an AC-to-DC converter wherein:

said synchronous rectifier controller connected only to circuits on a secondary winding of a transformer of said AC-to-DC converter and responding to a voltage of secondary winding for controlling a synchronous rectifier (SR) switch on said secondary side for generating a DC output signal.

14. The synchronous rectifier controller of claim 13 wherein:

said SR switch comprising a MOSFET transistor having a gate connected to said synchronous rectifier controller.

15. The synchronous rectifier controller of claim 14 wherein:

said SR switch comprising a N-channel MOSFET transistor having a gate connected to said synchronous rectifier controller for turning off said MOSFET when a drain of said N-channel MOSFET transistor is driven high.

ABSTRACT

The present invention discloses an AC-to-DC converter that includes a transformer having a primary side for inputting an input signal and a secondary side for outputting an output signal. The AC-to-DC converter further includes a synchronous rectifier controller connected to the secondary side for controlling a synchronous rectifier (SR) switch on the secondary side for generating the output signal. The SR switch is implemented as a MOSFET transistor with a gate connected to the synchronous rectifier controller. The synchronous rectifier controller further includes a plurality of circuit elements for turning off the SR switch before a main switch of the transformer is turned on. The synchronous rectifier controller further turns on the SR switch when the main switch of the transformer is turned off. The synchronous rectifier controller controls the SR switch and turns it off with a precisely controlled dead time before the main switch of the transformer is turned on.

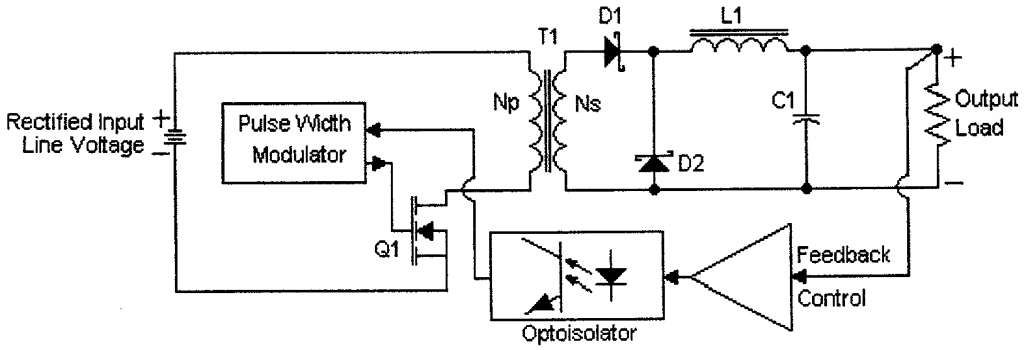


Fig. 1: Basic Forward Switching Converter Topology

Reference	Description		Reference	Description
Q1	Main Switching Transistor		T1	Transformer
D1	Forward Output Diode		D2	Freewheel Output Diode
L1	Output Filter Inductor		C1	Output Filter Capacitor

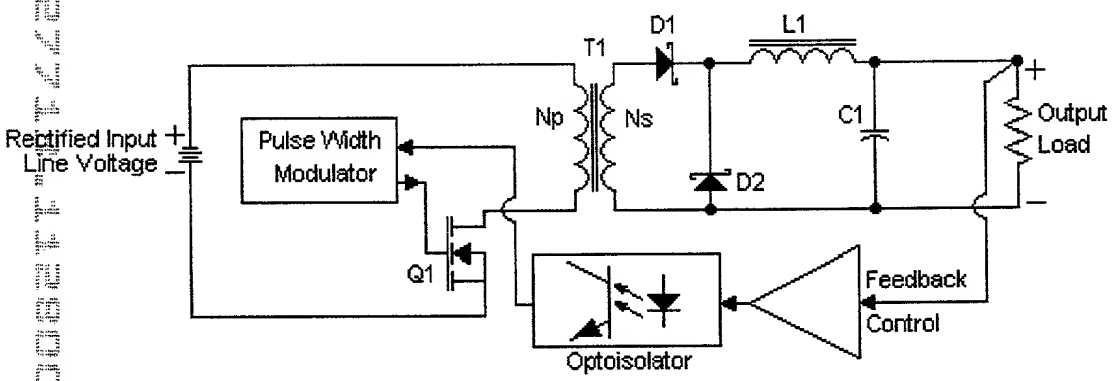


Fig. 1A: Basic Forward Switching Converter Topology Using Schottky Rectifiers

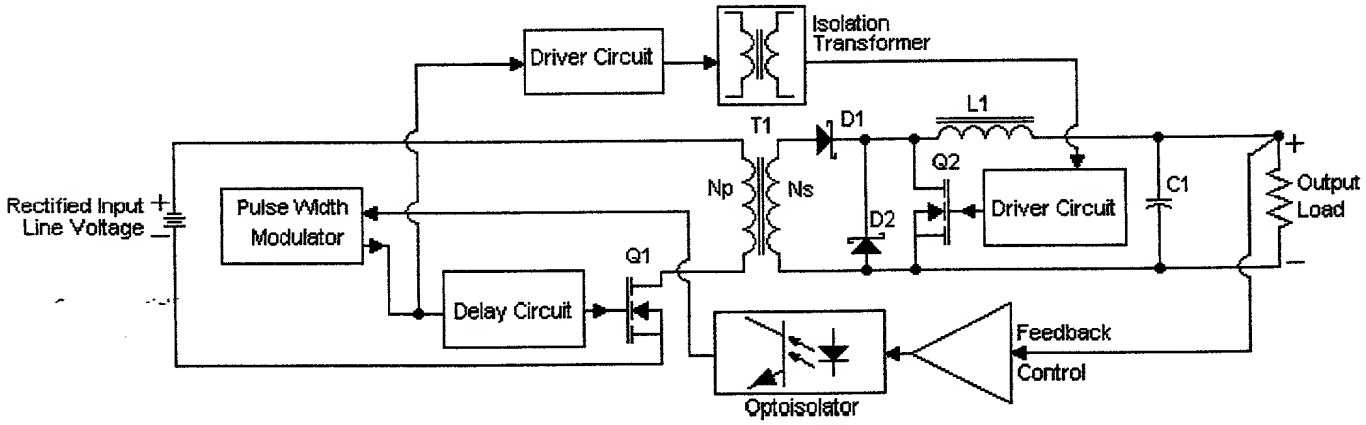


Fig. 1B: Synchronous-Rectified Converter with Primary Side Control; Prior Art

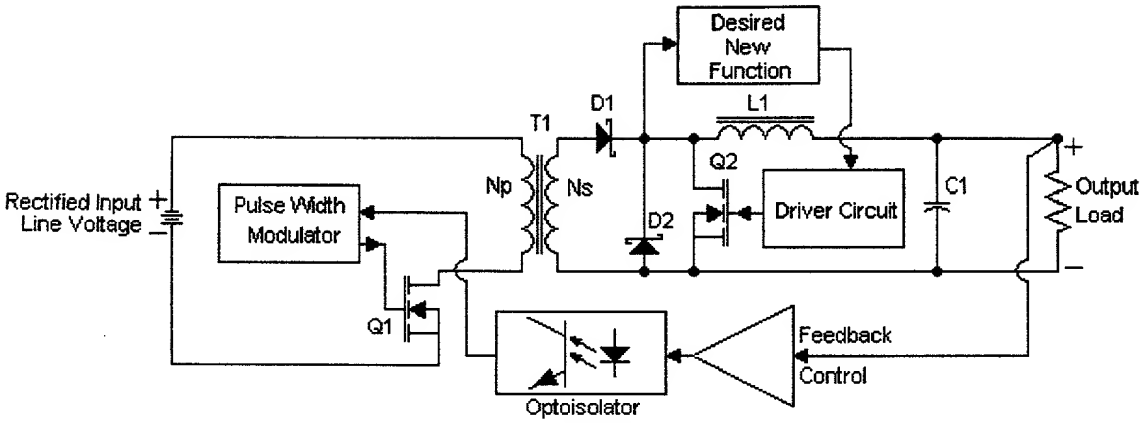


Fig. 2: Synchronous-Rectified Converter showing Desired New Control Function

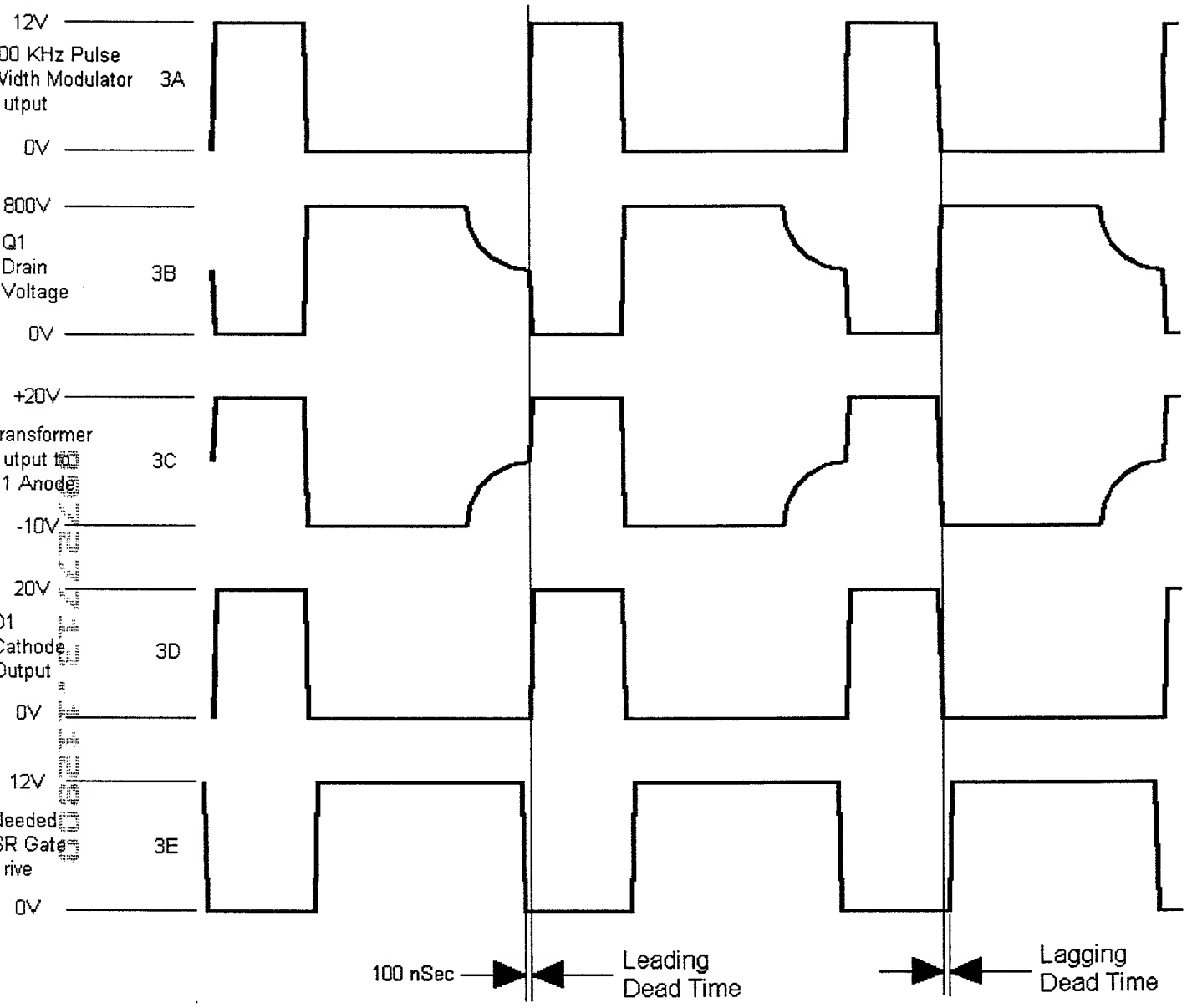


Fig. 3: Synchronous Rectifier Timing Diagram

is desirable to have a circuit which can drive the SR without the drawbacks listed above. The proposed new design would se timing information from the output of T1, D1 and would look like Fig. 5 shown below:

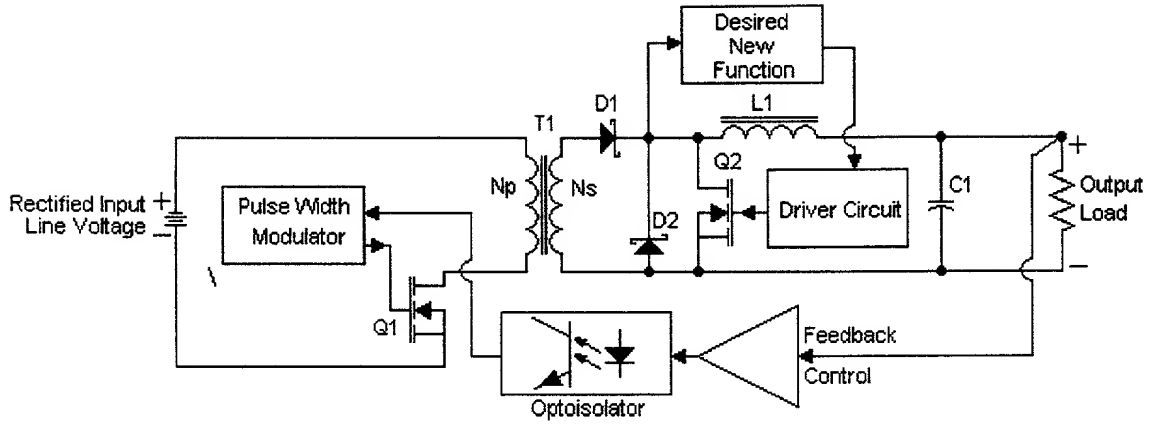


Fig. 4: Synchronous-Rectified Converter showing Desired New Control Function

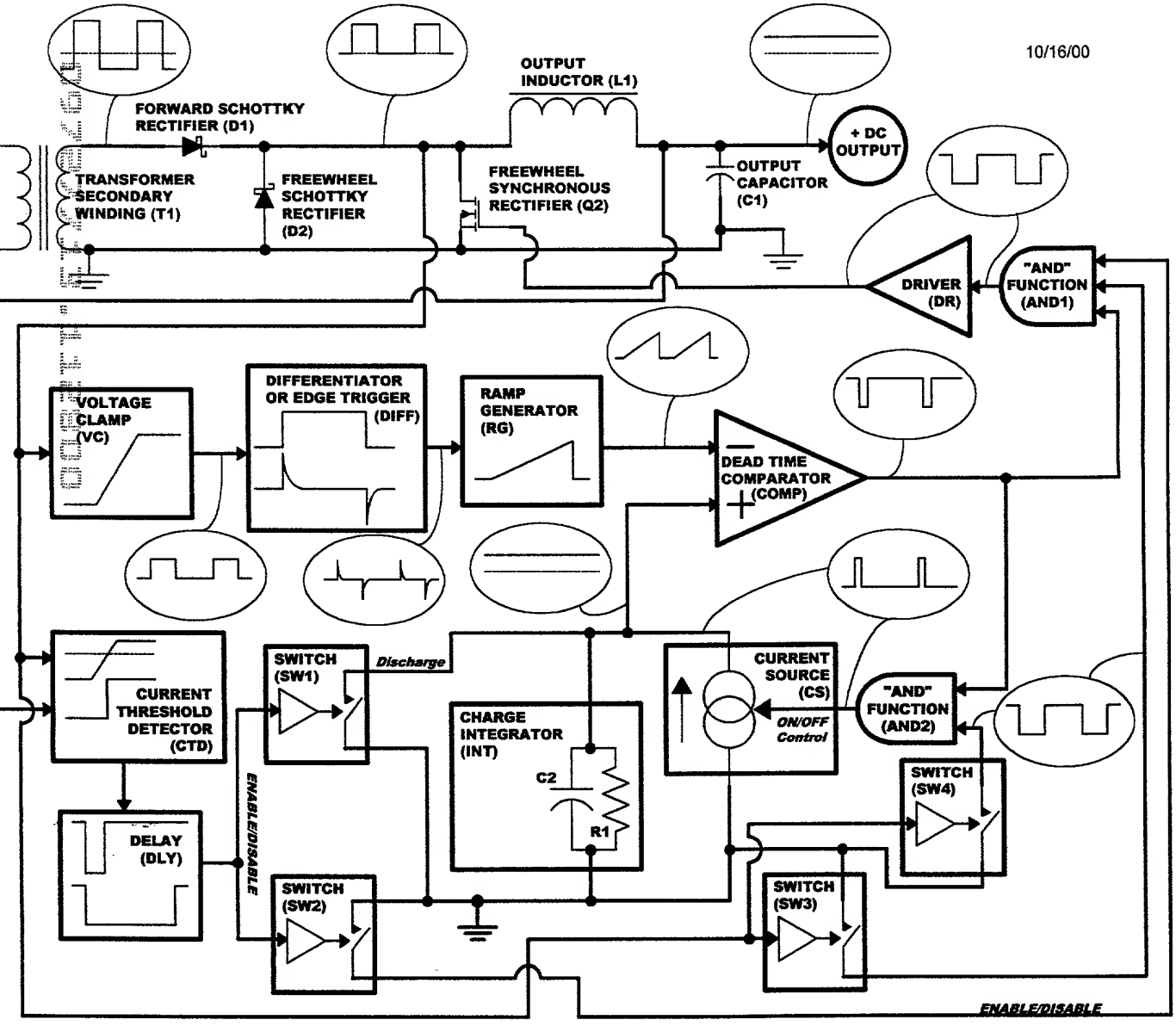


Figure 5: Block Diagram of Synchronous Rectifier System

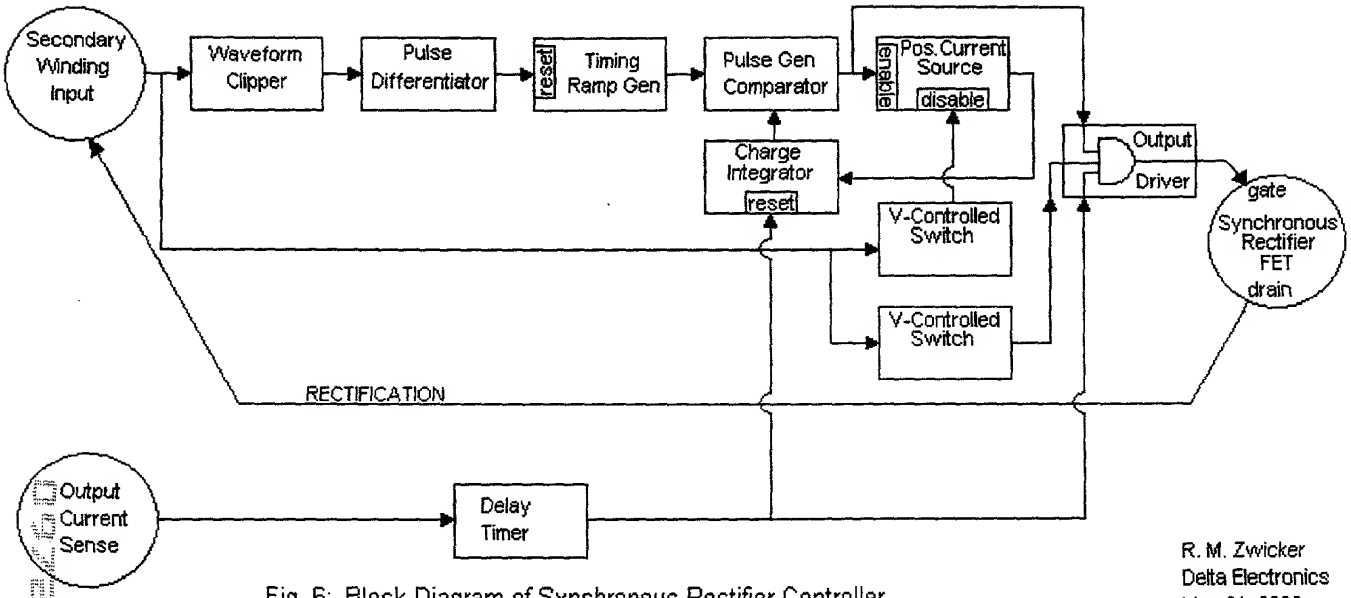


Fig. 6: Block Diagram of Synchronous Rectifier Controller

R. M. Zwicker
Delta Electronics
May 31, 2000

I had intended to discard this old Fig. 6. Did you want to use it as 5A or 5B?

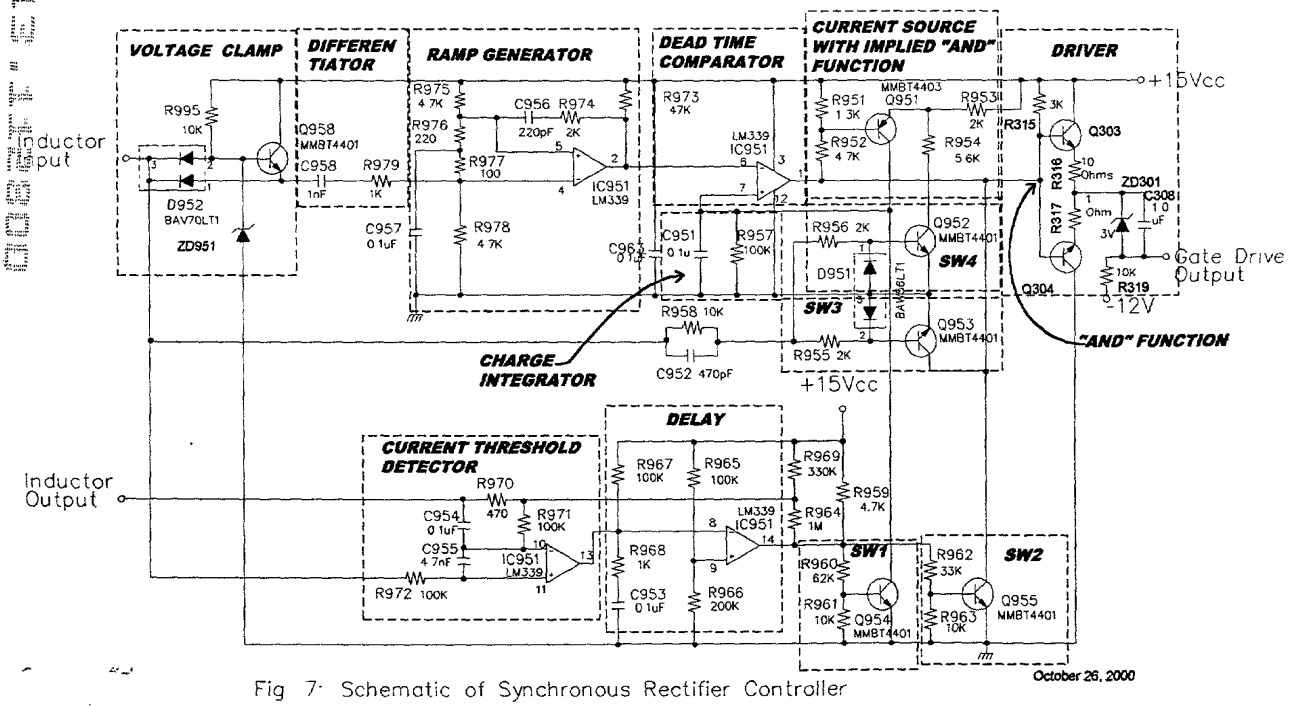


Fig 7: Schematic of Synchronous Rectifier Controller

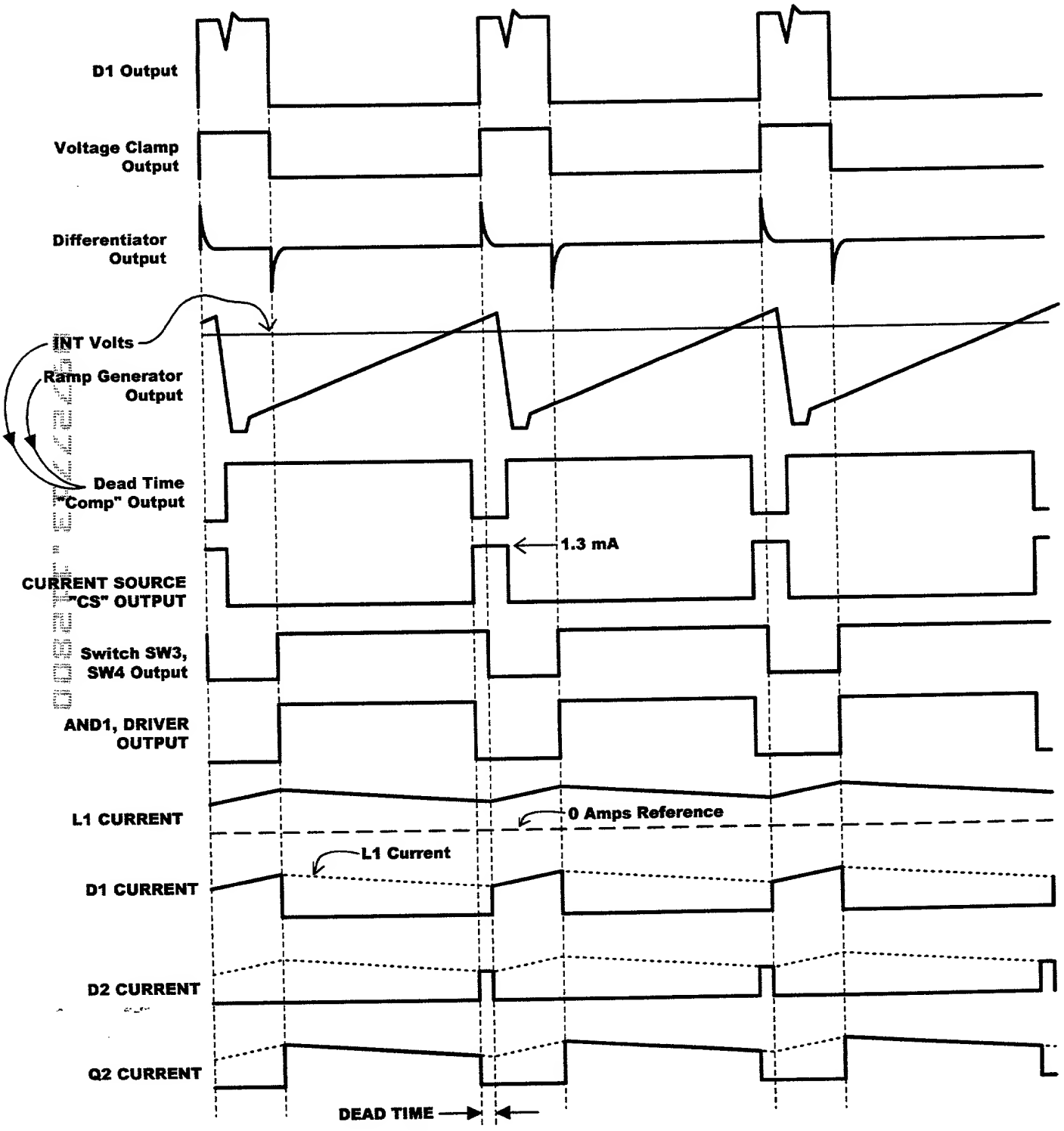


FIGURE 8. CIRCUIT TIMING DIAGRAM

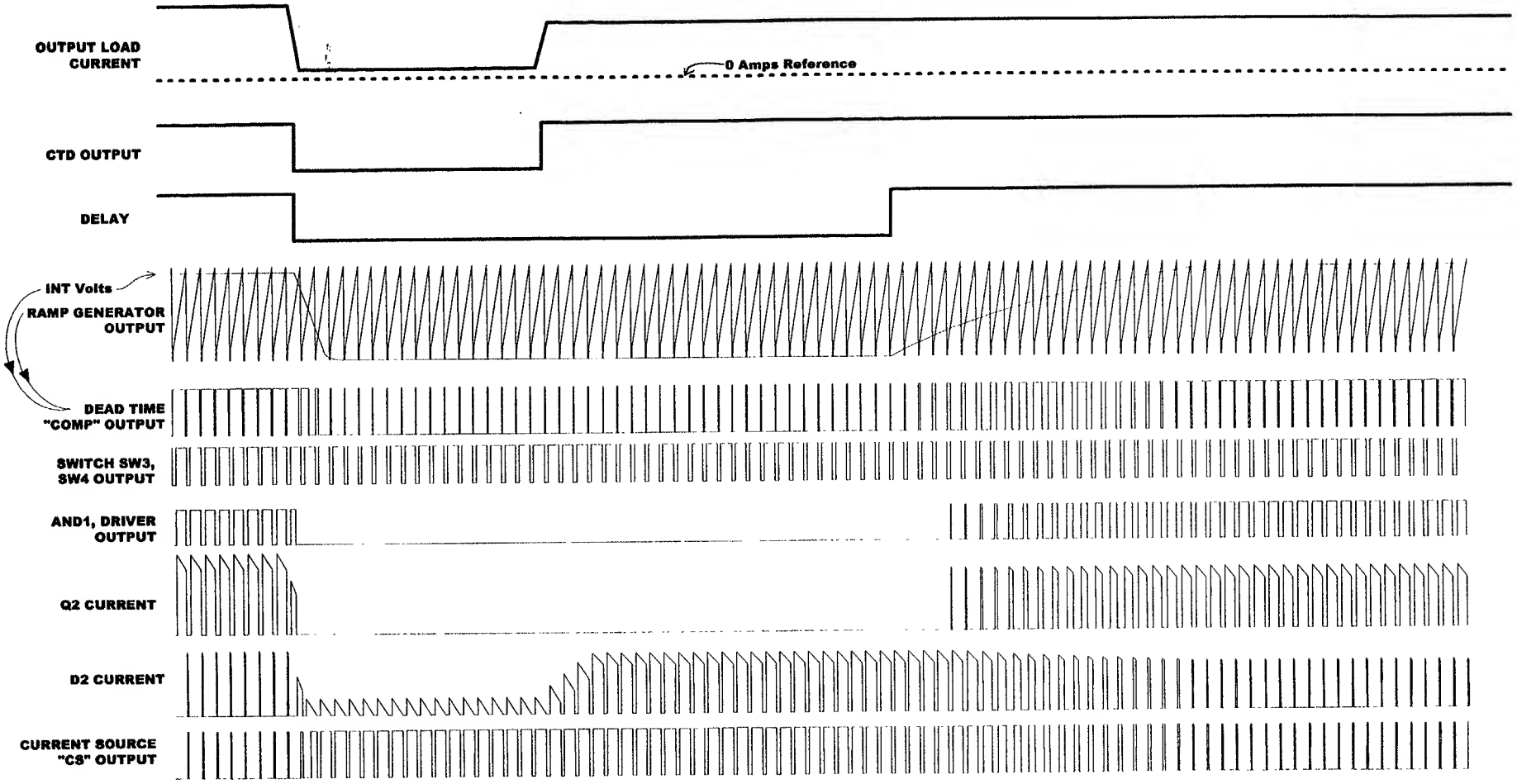


FIGURE 9. ENABLE/DISABLE TIMING DIAGRAM

Docket No.DELTA2K01

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

TITLE: SYNCHRONOUS RECTIFIER CONTROLLER FOR POWER SUPPLY SYSTEMS WITH HIGH POWER SWITCH AND HIGH EFFICIENCY

the specification of which (check one)
_X_ is attached hereto.
__ was filed on_____as Application Serial No._____and was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, ¤1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code ¤119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)
Priority Claimed

_____ _____ _____ __Yes __No
(Number) (Country) (Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, ¤120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, ¤112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, ¤1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ _____ _____
(Application Serial No.) (Filing Date) (Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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Docket No. DELTA2K01

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

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Inventor's signature: Date:

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